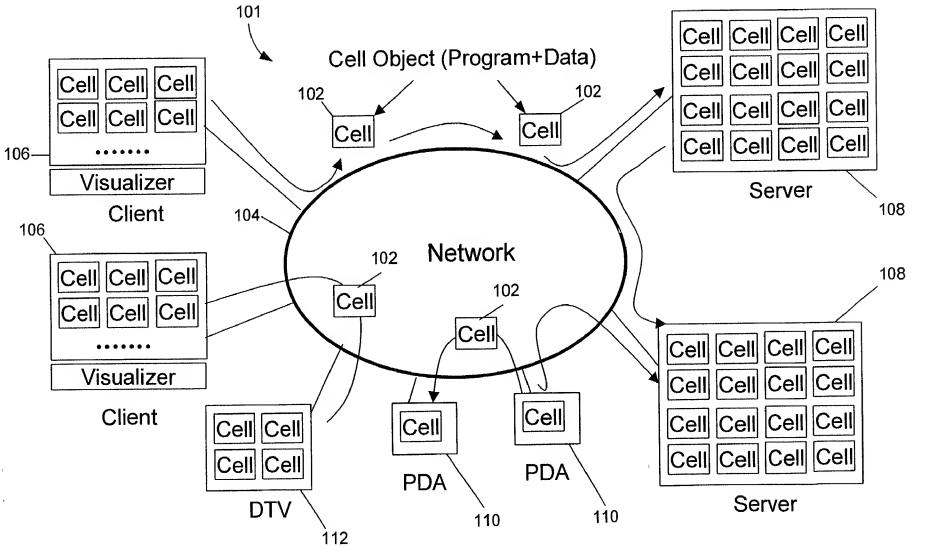
101
Cell Object (Program+Data)
102
102
Cell
Cell
Cell Cell Cell
Cell Cell Cell
106
Visualizer
Client
104
Network
Cell Cell Cell Cell
Cell Cell Cell Cell
Cell Cell Cell Cell
Cell Cell Cell Cell
Server
108
106
Cell Cell Cell
Cell Cell Cell
Visualizer
Client
102
102
Cell
Cell
108
Cell Cell Cell Cell
Cell Cell Cell Cell
Cell Cell Cell Cell
Cell Cell Cell Cell
Server
Cell Cell
Cell Cell
DTV
112
Cell
PDA
110
Cell
PDA
110

FIG. 1

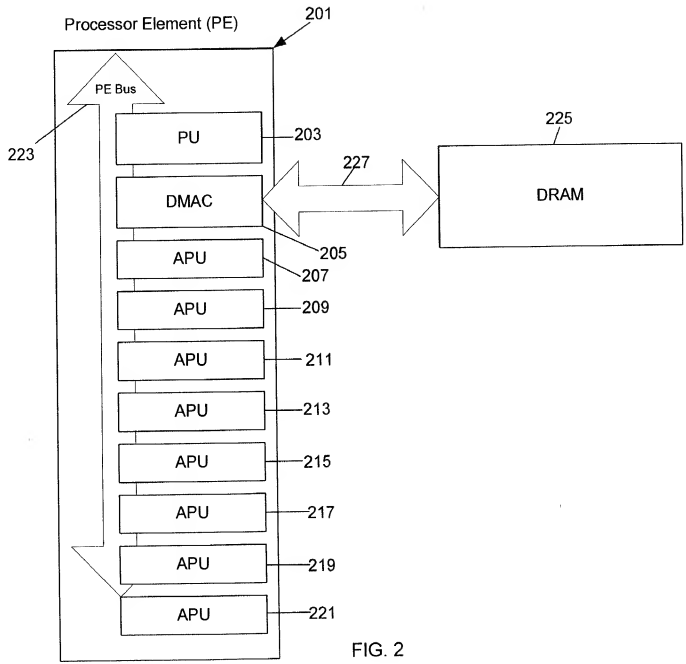
Processor Element (PE)
201
PE Bus
223
PU
203
DMAC
205
227
225
DRAM
APU
207
APU
209
APU
211
APU
213
APU
215
APU
217
APU
219
APU
221

FIG. 2

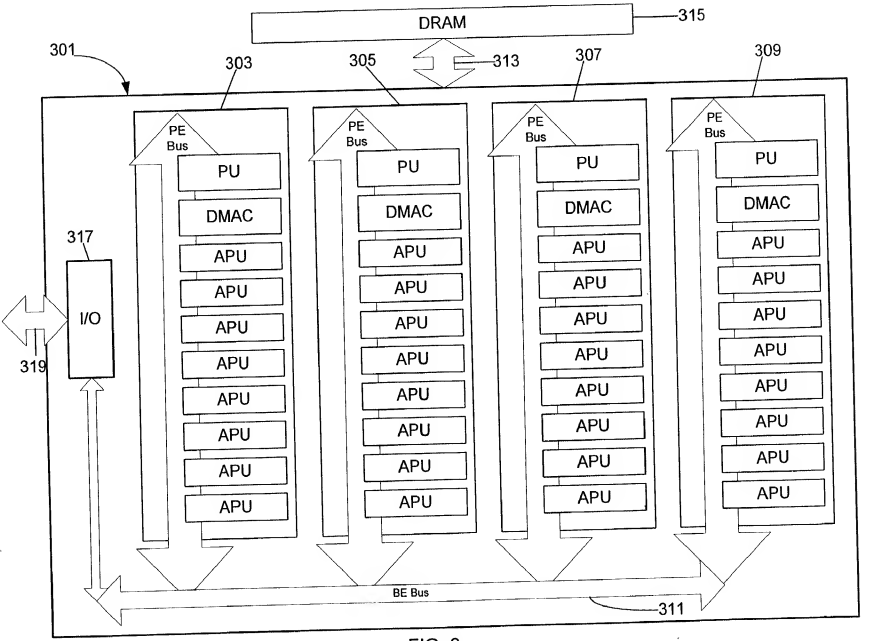

FIG. 3

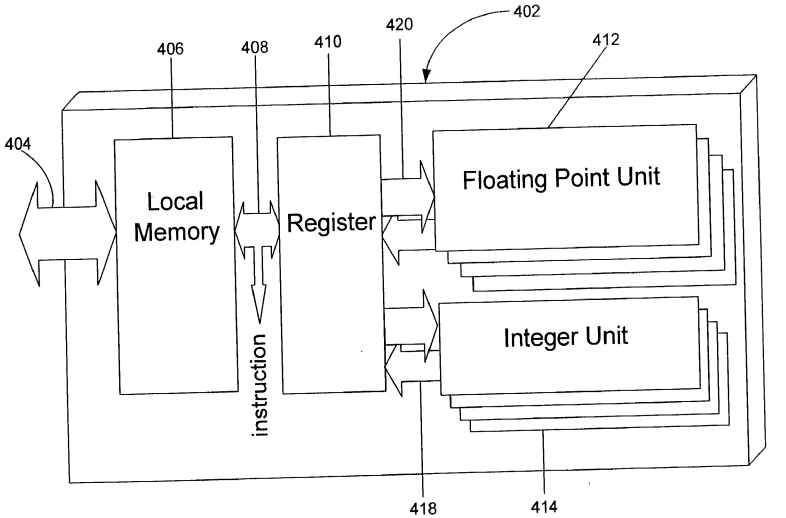

FIG. 4

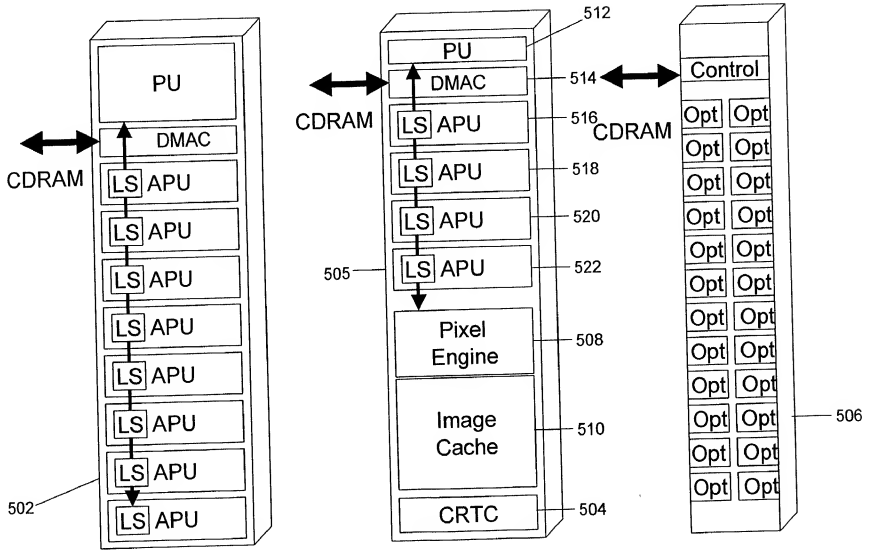
PU
DMAC
CDRAM
LS APU
LS APU
LS APU
LS APU
LS APU
LS APU
LS APU
LS APU
502
PU
DMAC
CDRAM
LS APU
LS APU
LS APU
LS APU
505
Pixel Engine
Image Cache
CRTC
512
514
516
518
520
522
508
510
504
Control
CDRAM
Opt
506

FIG. 5

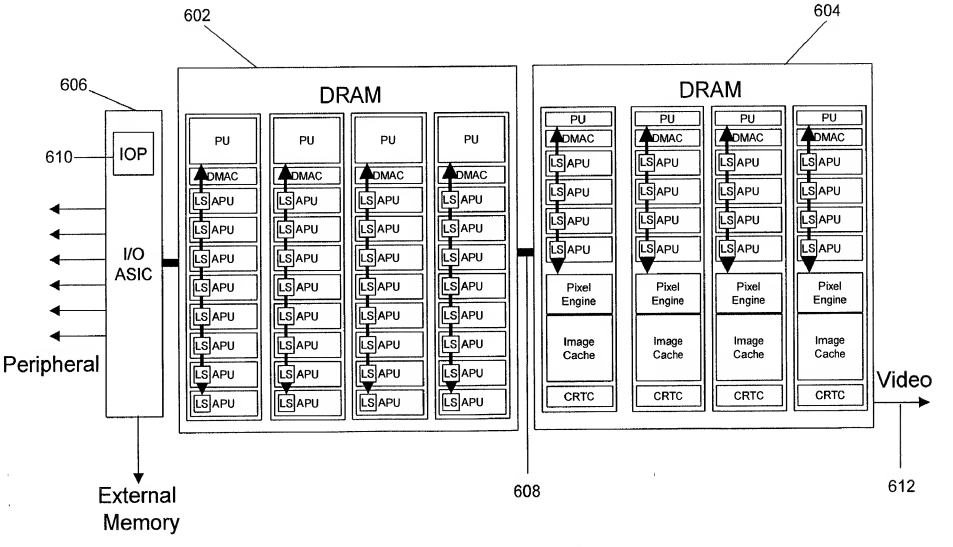

FIG. 6

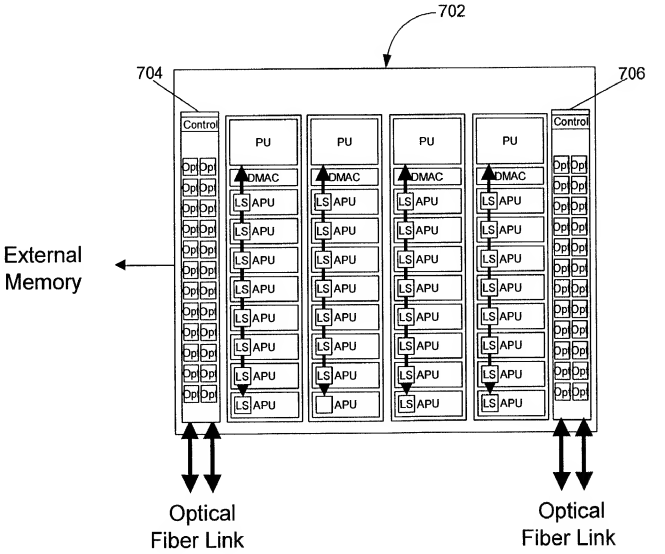

FIG. 7

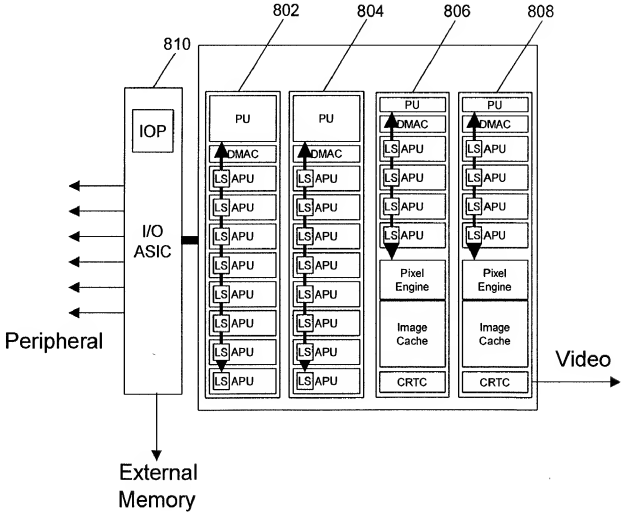

FIG. 8

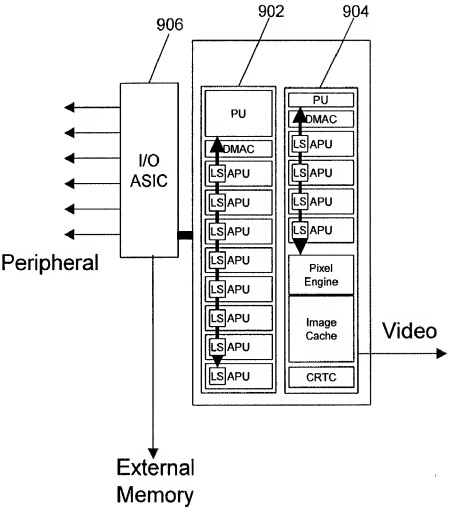

FIG. 9

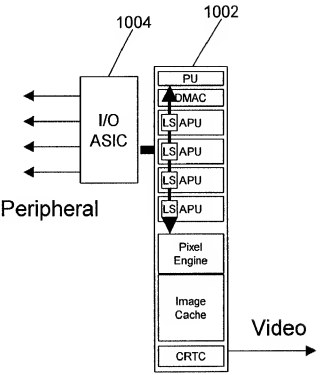

FIG. 10

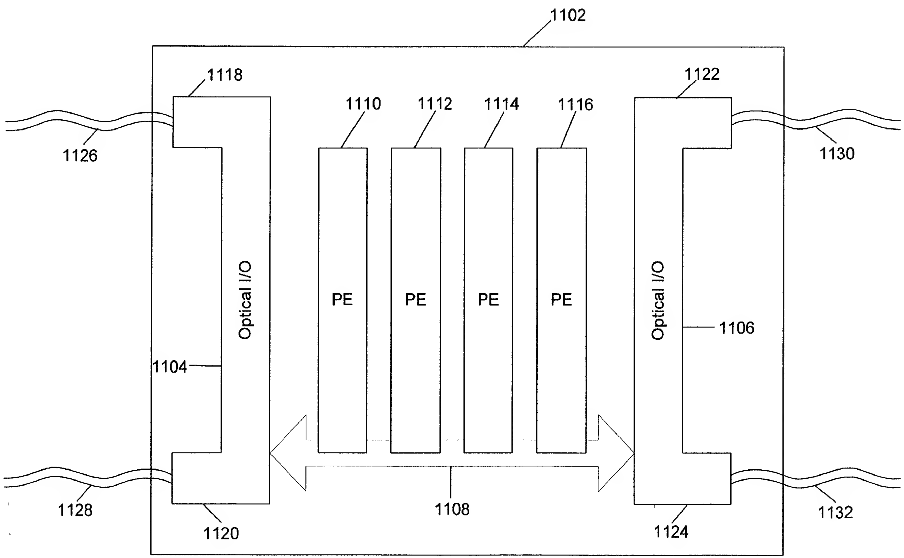
1102
1118
1122
1110
1112
1114
1116
1126
1130
PE
PE
PE
PE
Optical I/O
Optical I/O
1104
1106
1128
1108
1132
1120
1124

FIG. 11A

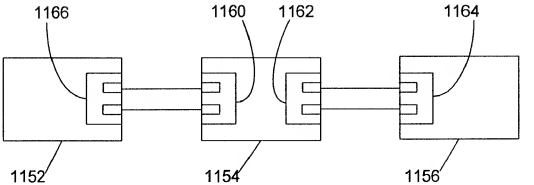

FIG. 11B

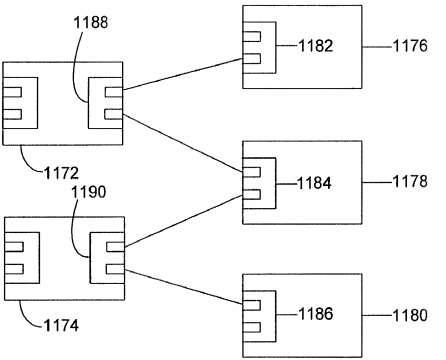

FIG. 11C

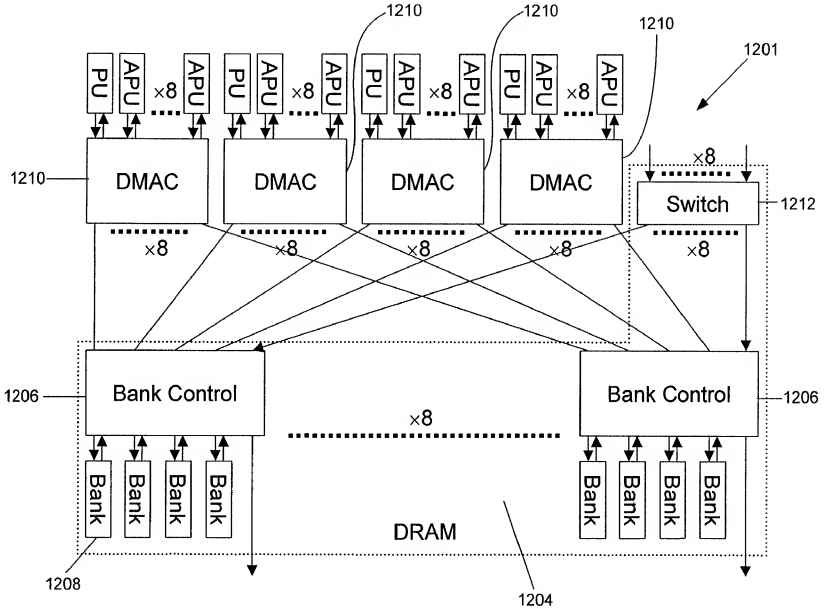
1210
1210
1210
1201
PU
APU
×8
APU
DMAC
DMAC
DMAC
DMAC
1210
×8
Switch
1212
×8
×8
×8
×8
×8
1206
Bank Control
Bank Control
1206
×8
Bank
Bank
Bank
Bank
Bank
Bank
Bank
Bank
DRAM
1208
1204

FIG. 12A

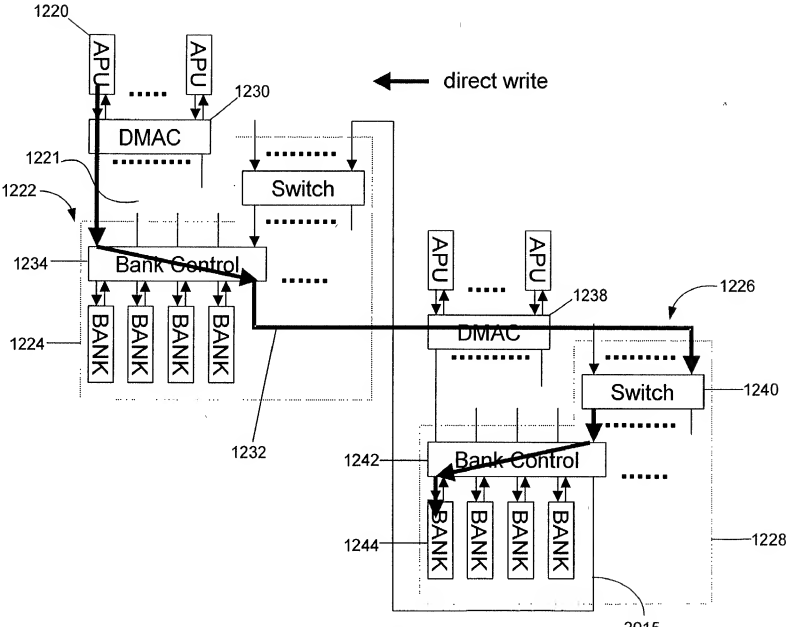
1220
APU
APU
1230
direct write
DMAC
1221
Switch
1222
1234
Bank Control
BANK
BANK
BANK
BANK
1224
1232
APU
APU
1238
1226
DMAC
Switch
1240
1242
Bank Control
BANK
BANK
BANK
BANK
1244
1228
2015

FIG. 12B

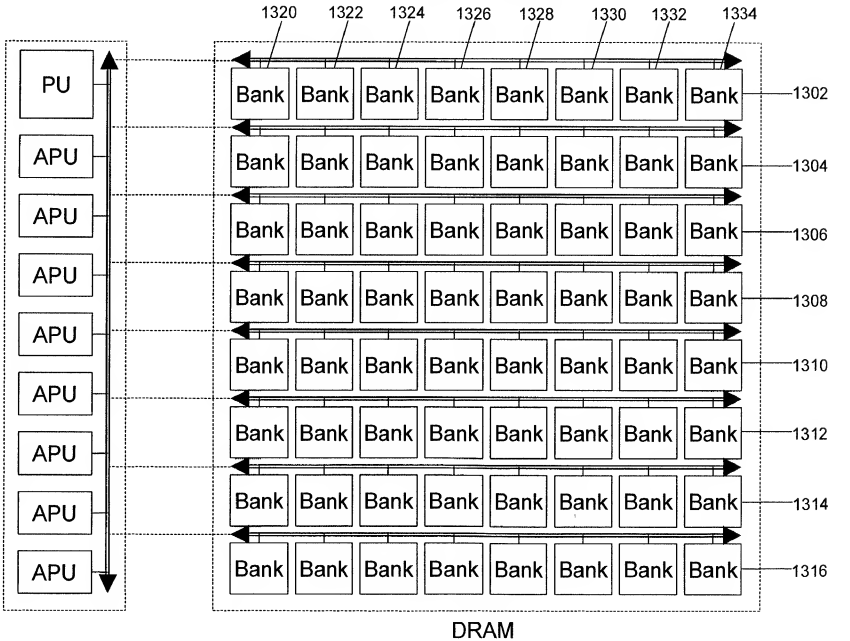
1320
1322
1324
1326
1328
1330
1332
1334
PU
APU
APU
APU
APU
APU
APU
APU
APU
Bank
1302
1304
1306
1308
1310
1312
1314
1316
DRAM

FIG. 13

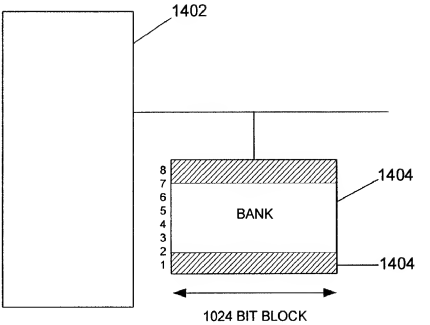

FIG. 14A

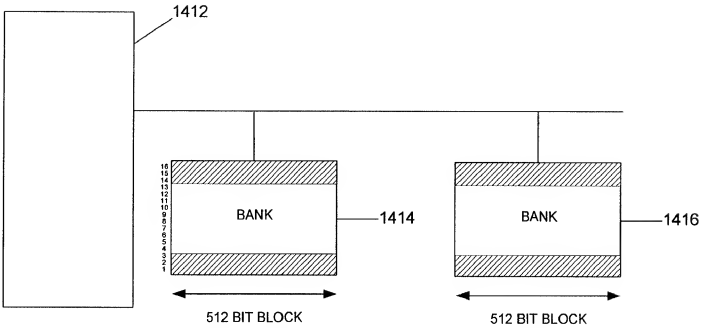
1412
16
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
BANK
1414
BANK
1416
512 BIT BLOCK
512 BIT BLOCK

FIG. 14B

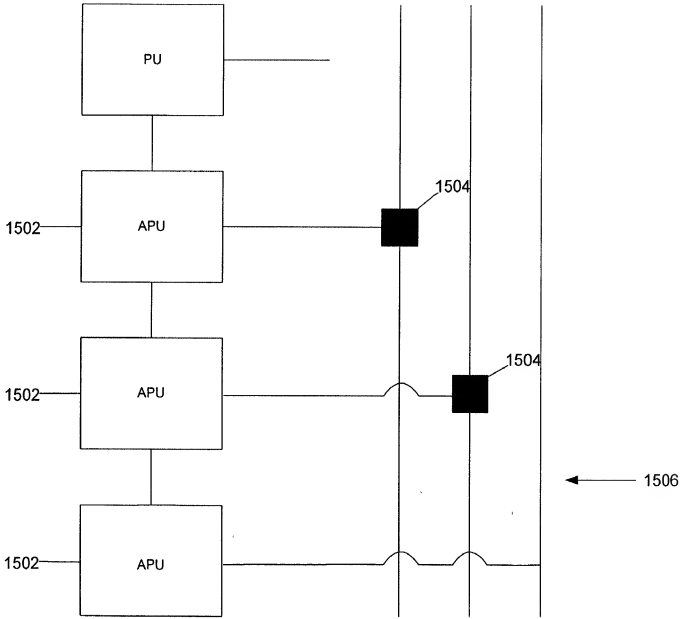

FIG. 15

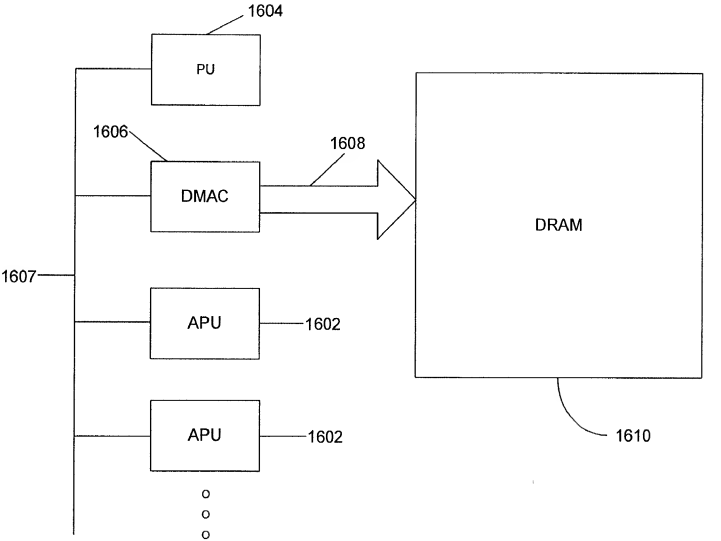

FIG. 16

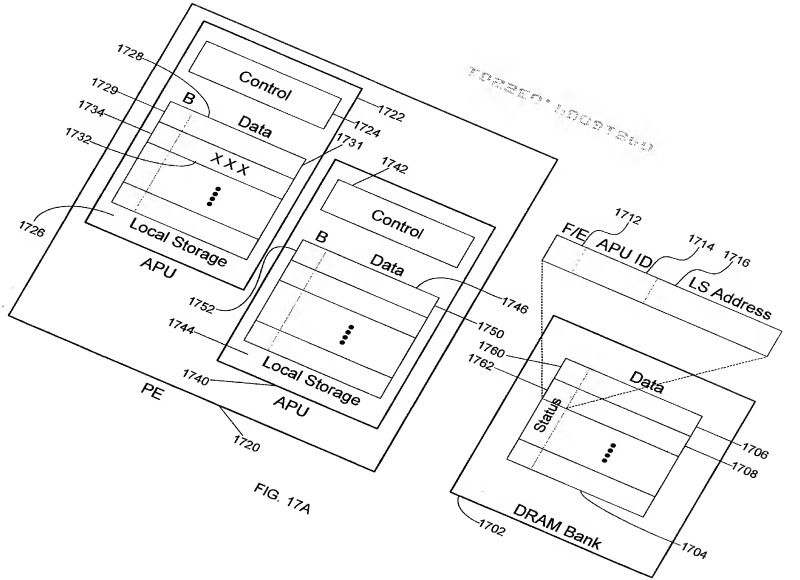
1728
1729
1734
1732
1726
Control
B
Data
XXX
Local Storage
APU
1722
1724
1731
1742
Control
B
Data
1752
1744
1746
1750
Local Storage
APU
1740
PE
1720
1712
F/E
APU ID
1714
1716
LS Address
1760
1762
Data
Status
1706
1708
DRAM Bank
1702
1704

FIG. 17A

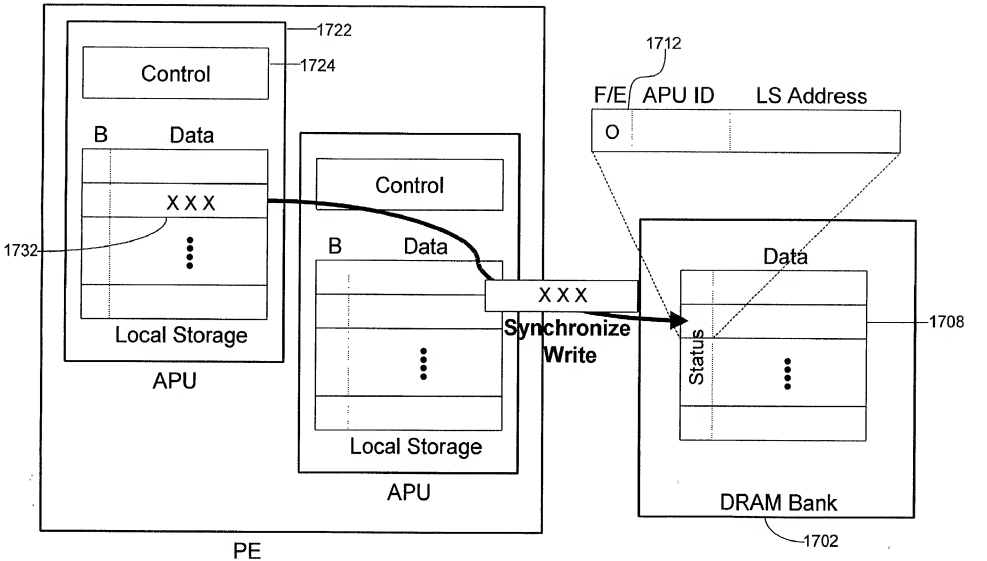
1722
Control
1724
B
Data
XXX
1732
Local Storage
APU
Control
B
Data
Local Storage
APU
PE
1712
F/E
APU ID
LS Address
O
XXX
Synchronize
Write
Data
Status
1708
DRAM Bank
1702

FIG. 17B

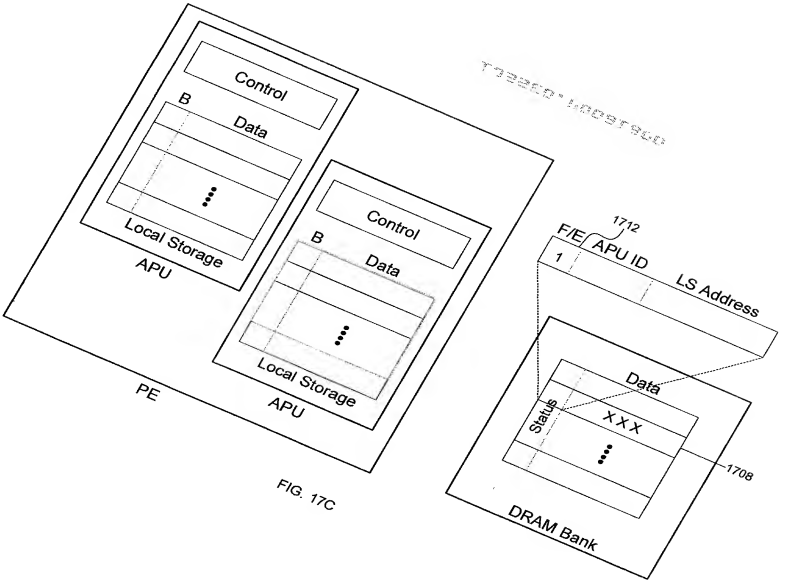
Control
B
Data
Local Storage
APU
Control
B
Data
Local Storage
APU
PE
1712
F/E
APU ID
LS Address
1
Data
Status
XXX
1708
DRAM Bank

FIG. 17C

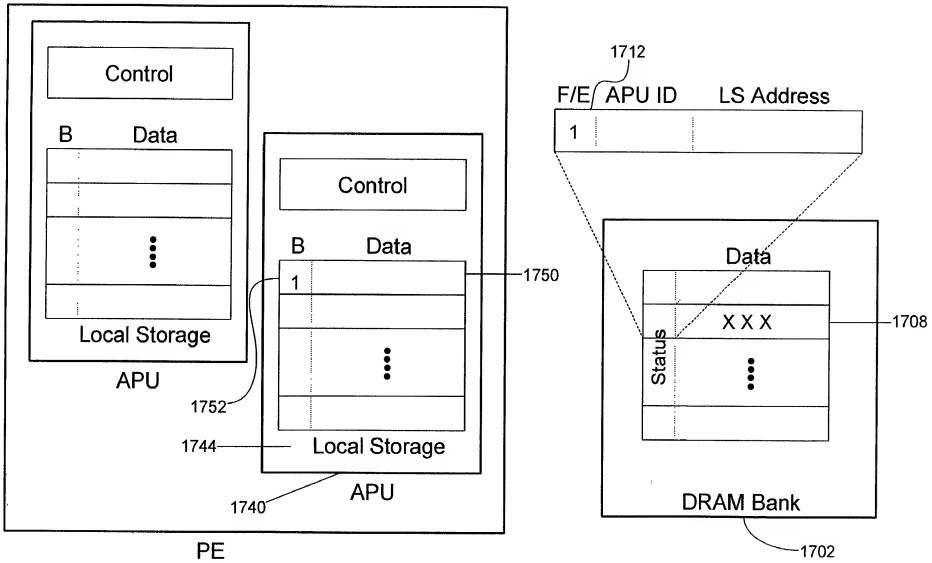

FIG. 17D

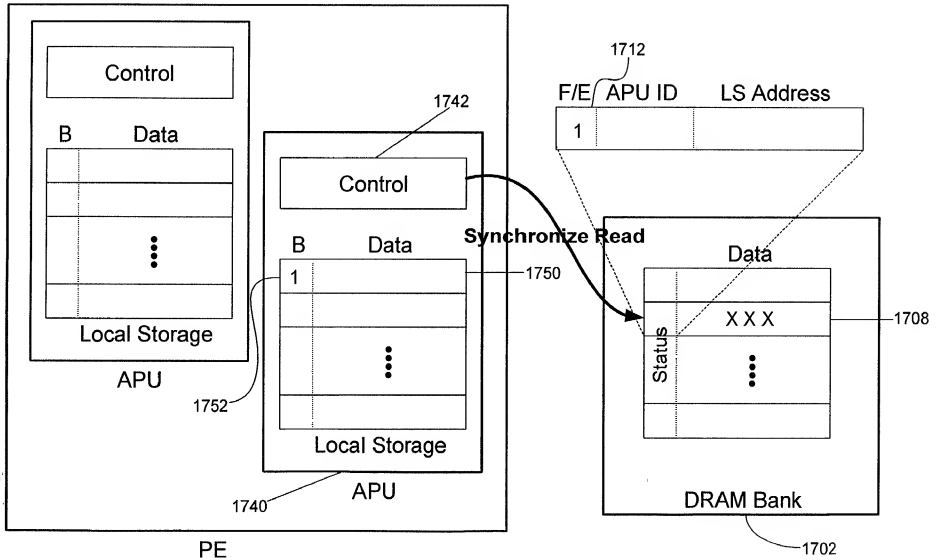

FIG. 17E

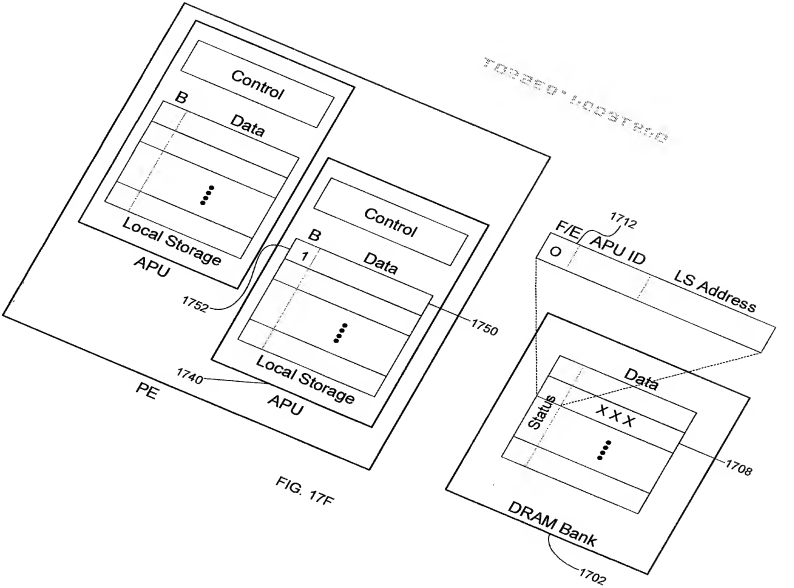
Control
B
Data
Local Storage
APU
1752
Control
B
1
Data
1750
Local Storage
APU
1740
PE
1712
F/E
APU ID
LS Address
O
Data
Status
XXX
1708
DRAM Bank
1702

FIG. 17F

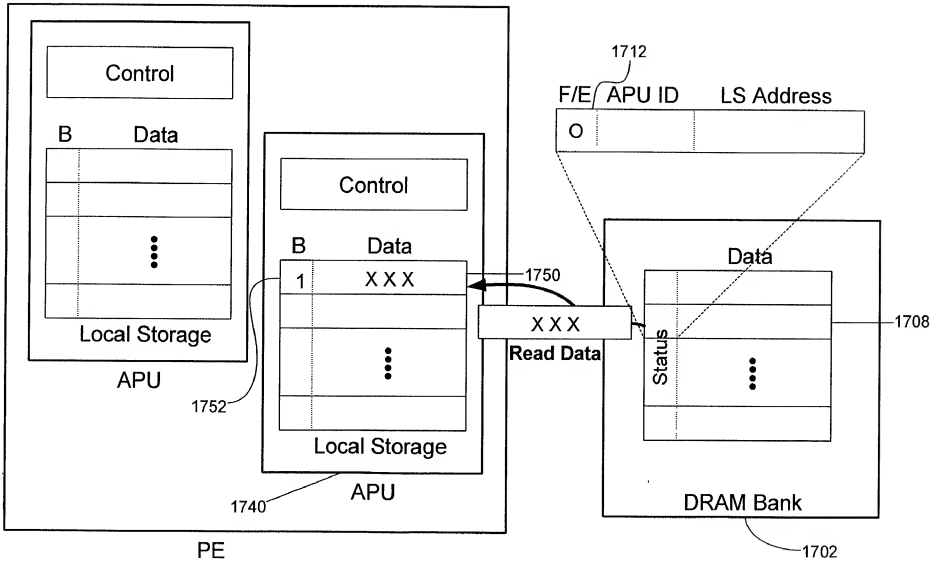
Control
B
Data
Local Storage
APU
Control
B
Data
1
X X X
1752
Local Storage
APU
1740
PE
1712
F/E
APU ID
LS Address
O
1750
X X X
Read Data
Data
Status
1708
DRAM Bank
1702

FIG. 17G

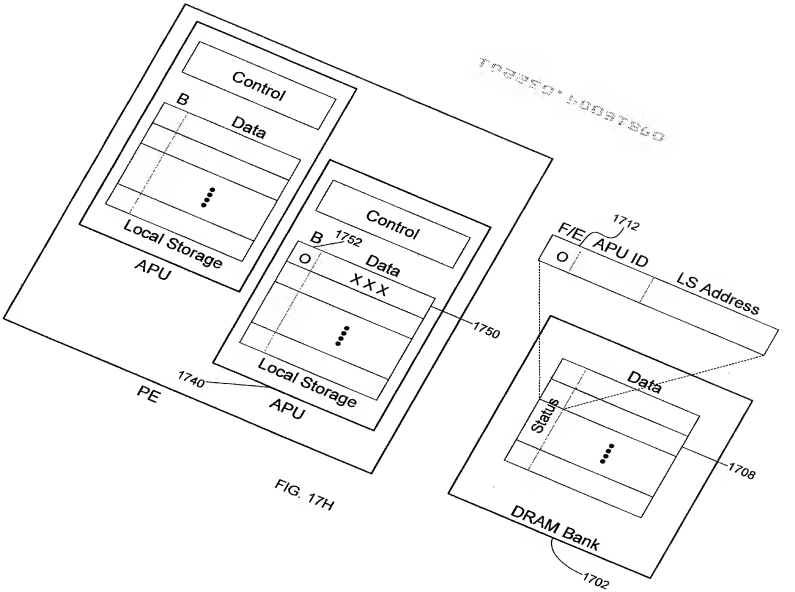
Control
B
Data
Local Storage
APU
Control
B
1752
O
Data
X X X
Local Storage
APU
1750
1740
PE
1712
F/E
APU ID
LS Address
O
Data
Status
1708
DRAM Bank
1702

FIG. 17H

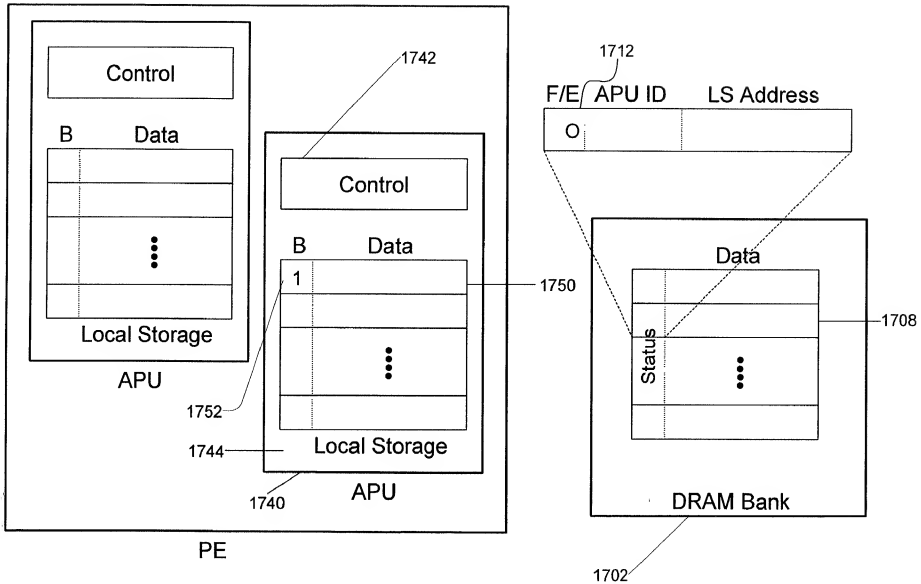
Control
B
Data
Local Storage
APU
1742
Control
B
Data
1
1750
1752
1744
Local Storage
1740
APU
PE
1712
F/E
APU ID
LS Address
O
Data
Status
1708
DRAM Bank
1702

FIG. 17I

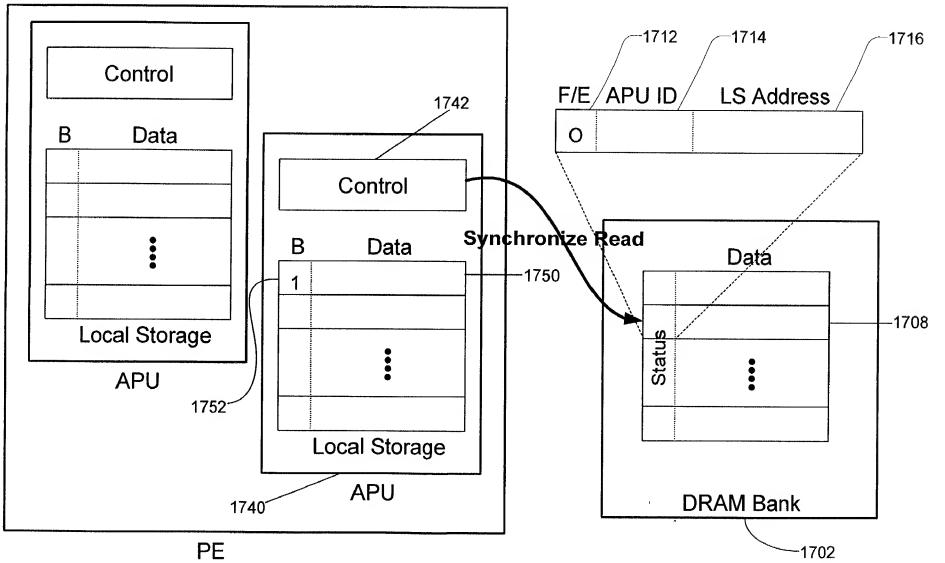
Control
B
Data
Local Storage
APU
PE
1742
Control
B
Data
1
1750
1752
Local Storage
APU
1740
Synchronize Read
1712
1714
1716
F/E
APU ID
LS Address
0
Data
Status
1708
DRAM Bank
1702

FIG. 17J

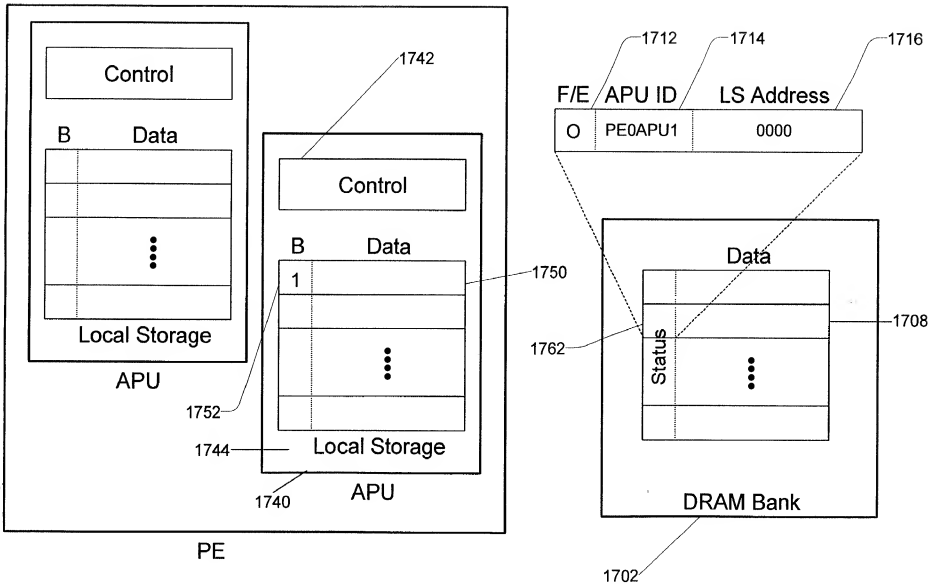
Control
B
Data
Local Storage
APU
1742
Control
B
Data
1
1750
1752
1744
Local Storage
1740
APU
PE
1712
1714
1716
F/E
APU ID
LS Address
O
PE0APU1
0000
Data
1708
1762
Status
DRAM Bank
1702

FIG. 17K

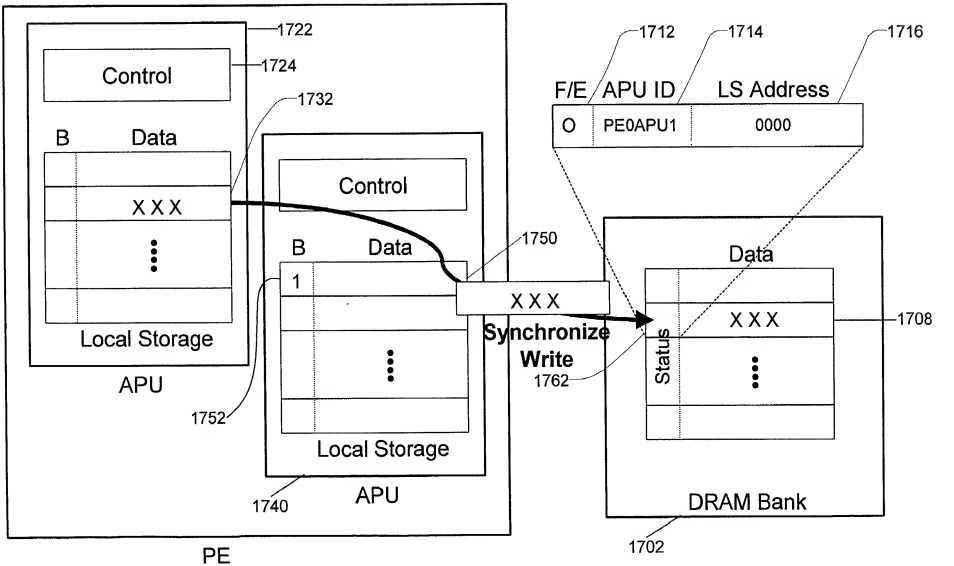
1722
Control
1724
1732
B
Data
X X X
Local Storage
APU
1752
Control
B
Data
1
Local Storage
APU
1740
PE
1712
1714
1716
F/E
APU ID
LS Address
O
PE0APU1
0000
1750
X X X
Synchronize
Write
1762
Data
X X X
Status
1708
DRAM Bank
1702

FIG. 17L

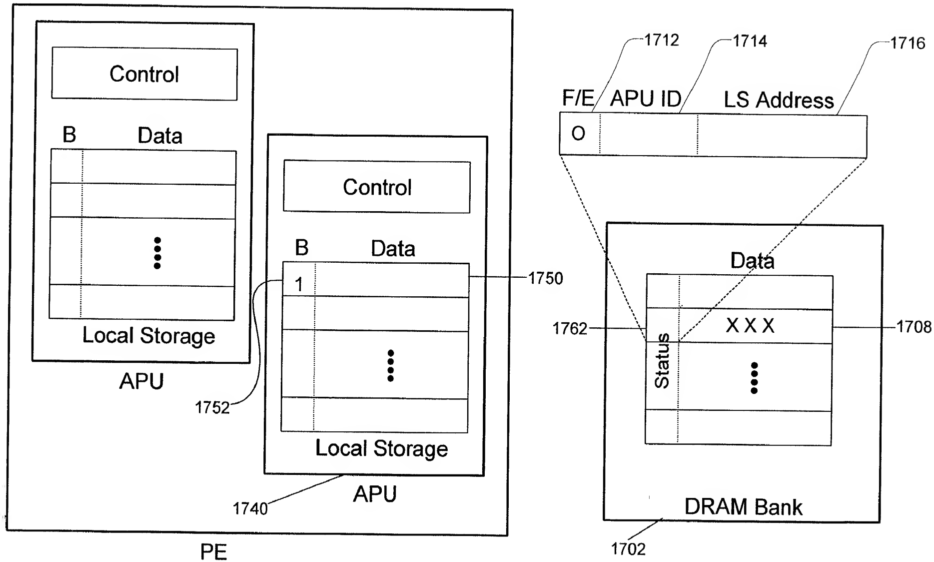
Control
B
Data
Local Storage
APU
Control
B
Data
1
Local Storage
APU
PE
1750
1752
1740
F/E
APU ID
LS Address
O
1712
1714
1716
Data
Status
X X X
DRAM Bank
1762
1708
1702

FIG. 17M

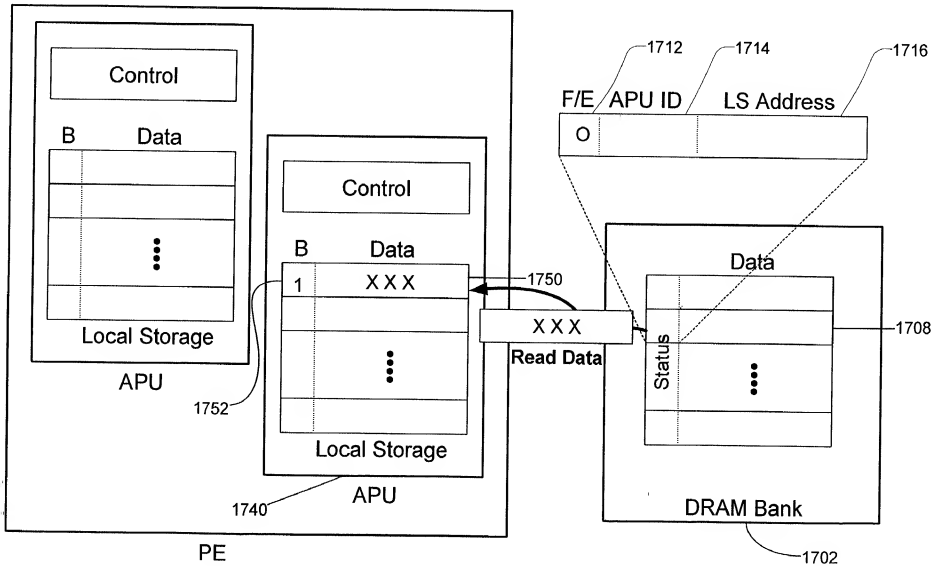
Control
B
Data
Local Storage
APU
Control
B
Data
1
X X X
Local Storage
APU
1740
PE
1752
1750
X X X
Read Data
1712
1714
1716
F/E
APU ID
LS Address
O
Data
Status
1708
DRAM Bank
1702

FIG. 17N

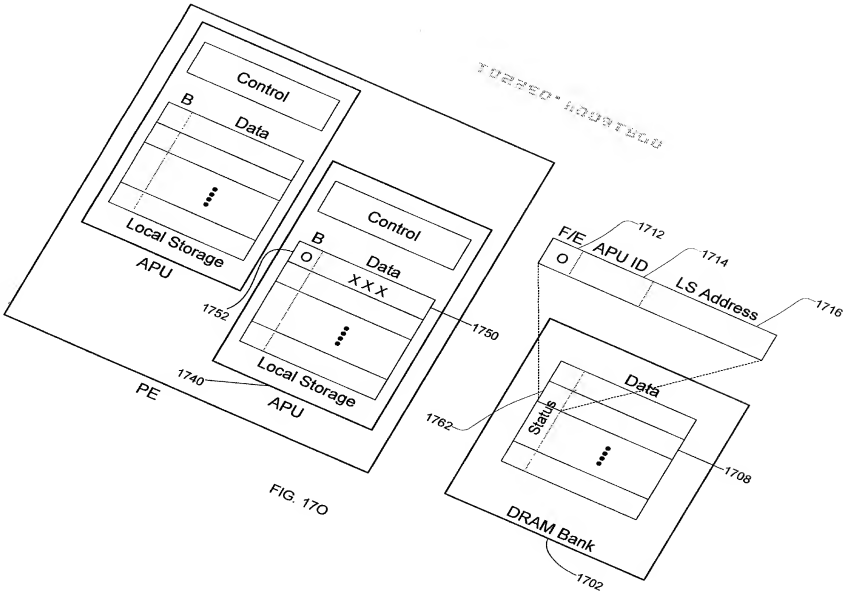
Control
B
Data
Local Storage
APU
Control
B
O
Data
XXX
Local Storage
APU
PE
1740
1752
1750
F/E
O
APU ID
LS Address
1712
1714
1716
Data
Status
1762
1708
DRAM Bank
1702

FIG. 17O

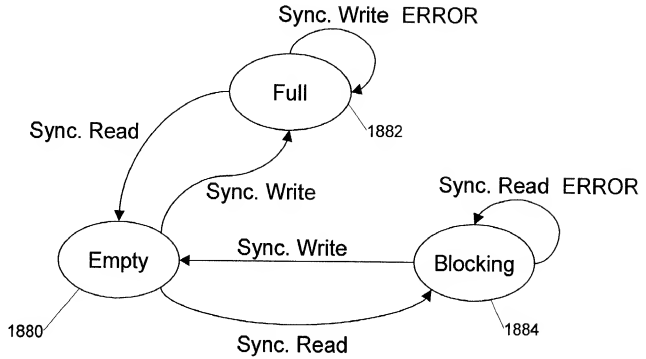
Sync. Write ERROR
Full
1882
Sync. Read
Sync. Write
Sync. Read ERROR
Empty
Sync. Write
Blocking
1880
1884
Sync. Read

FIG. 18

Key Control Table

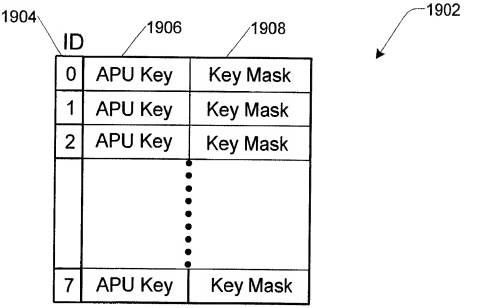

FIG. 19

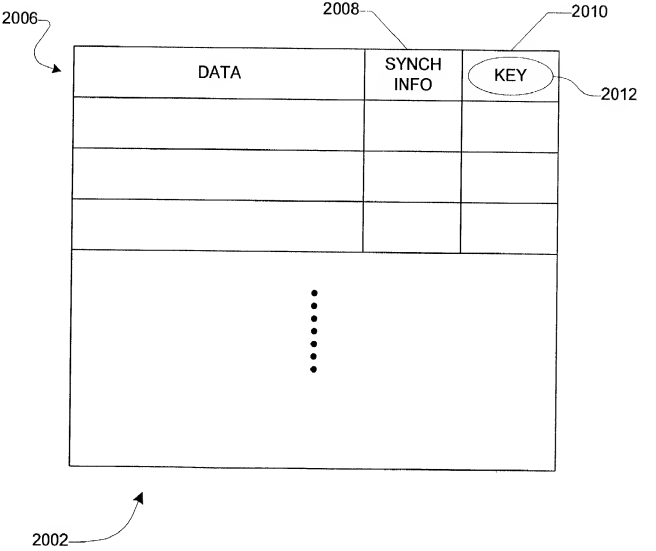

FIG. 20

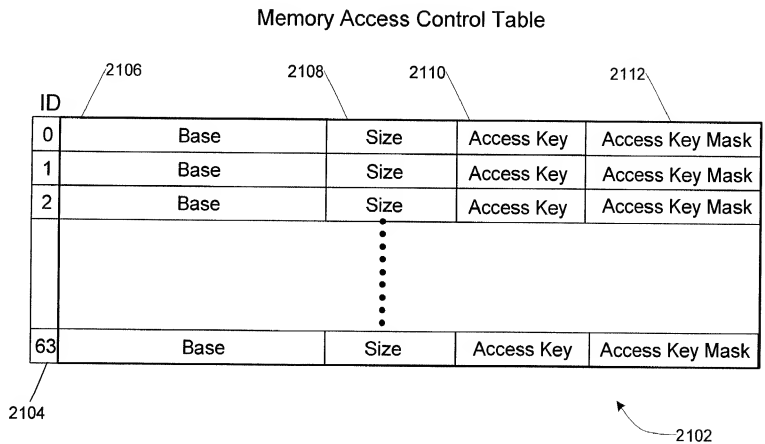
Memory Access Control Table
2106
2108
2110
2112
ID
0
Base
Size
Access Key
Access Key Mask
1
Base
Size
Access Key
Access Key Mask
2
Base
Size
Access Key
Access Key Mask
63
Base
Size
Access Key
Access Key Mask
2104
2102

FIG. 21

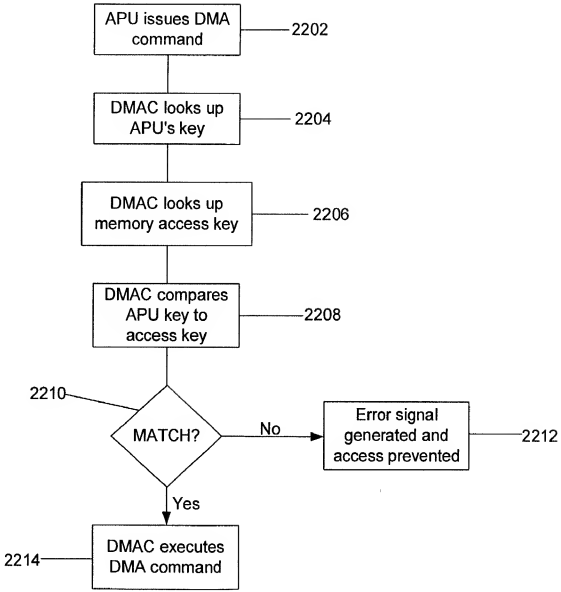
APU issues DMA command
2202
DMAC looks up APU's key
2204
DMAC looks up memory access key
2206
DMAC compares APU key to access key
2208
2210
MATCH?
No
Error signal generated and access prevented
2212
Yes
DMAC executes DMA command
2214

FIG. 22

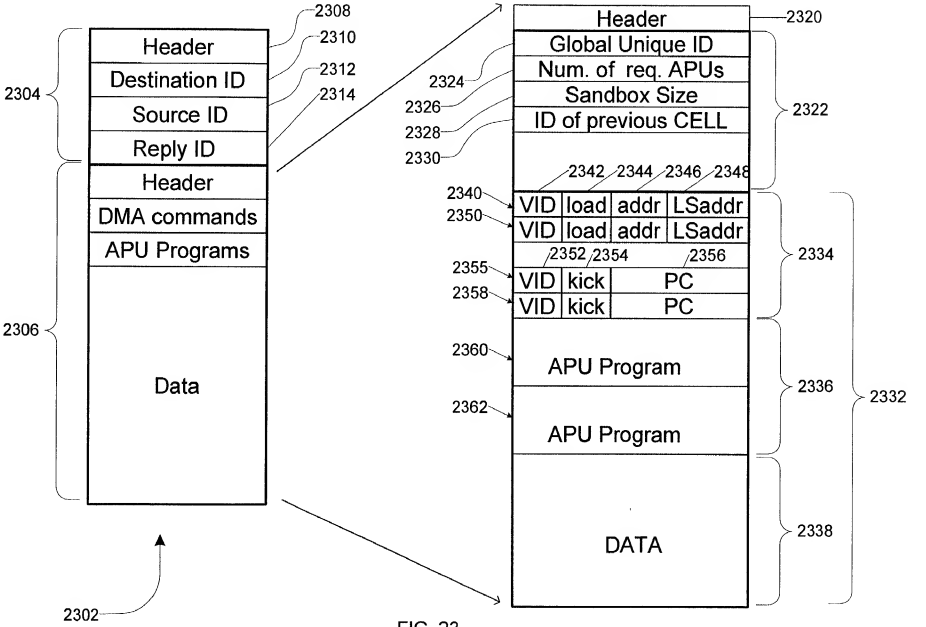
Header
Destination ID
Source ID
Reply ID
Header
DMA commands
APU Programs
Data
2302
2304
2306
2308
2310
2312
2314
Header
Global Unique ID
Num. of req. APUs
Sandbox Size
ID of previous CELL
2320
2322
2324
2326
2328
2330
2342
2344
2346
2348
2340
2350
VID load addr LSaddr
VID load addr LSaddr
2352
2354
2356
2355
2358
VID kick PC
VID kick PC
2334
2360
APU Program
2362
APU Program
2336
2332
DATA
2338

FIG. 23

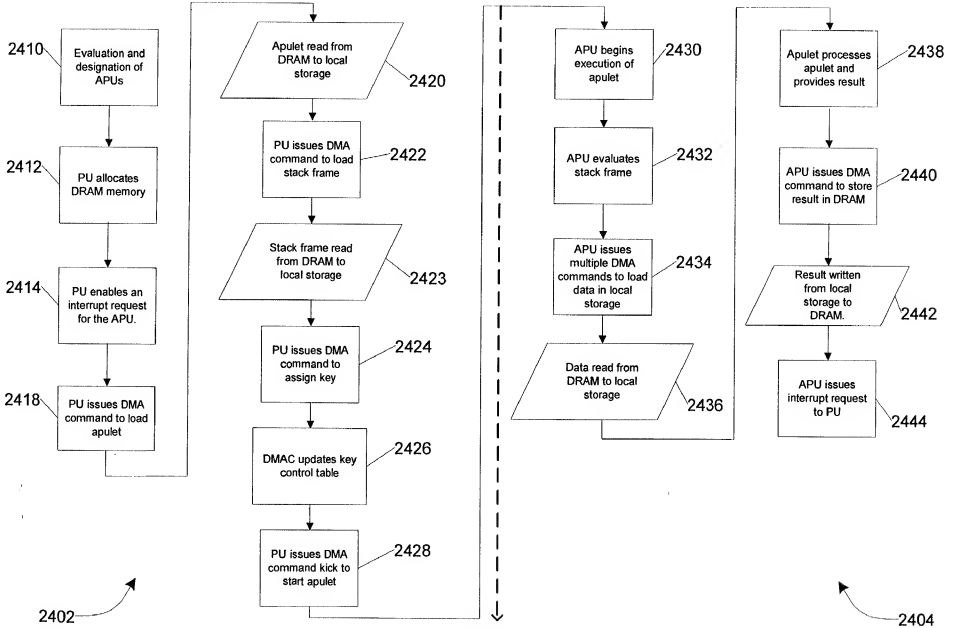

FIG. 24

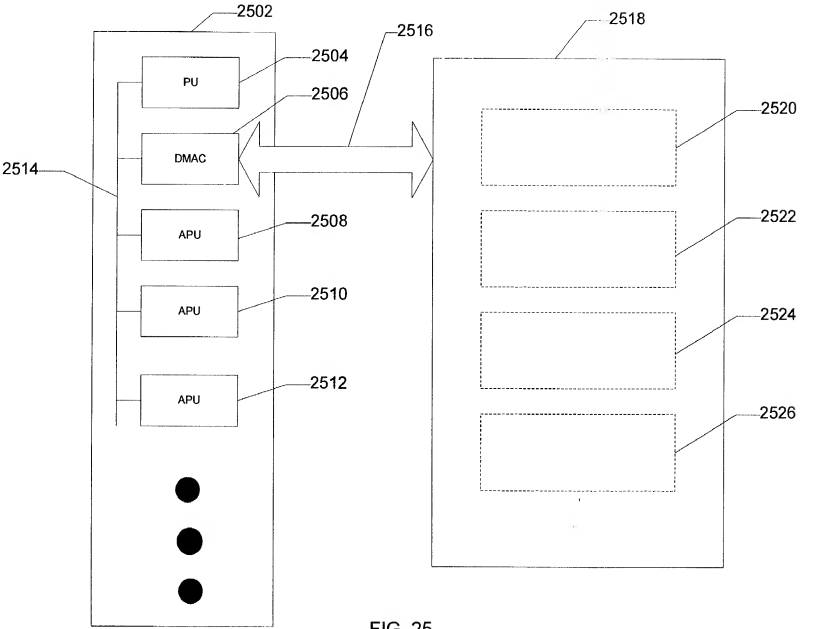

FIG. 25

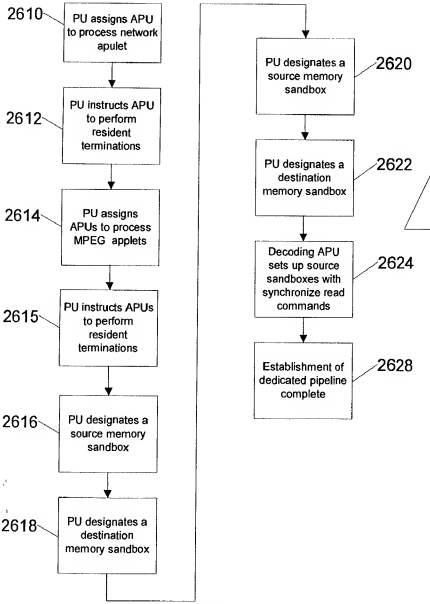

FIG. 26A

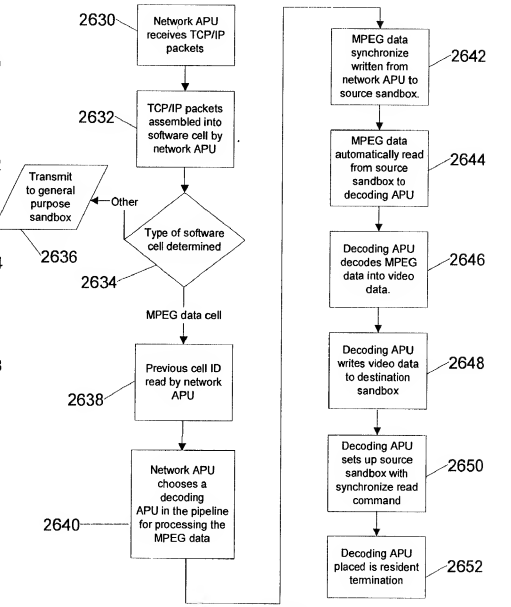

FIG. 26B

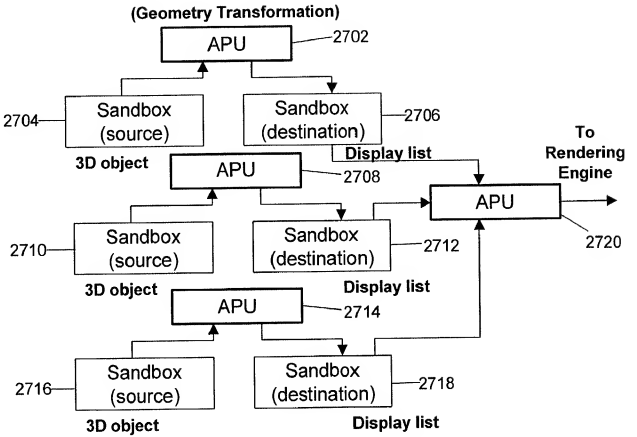

FIG. 27

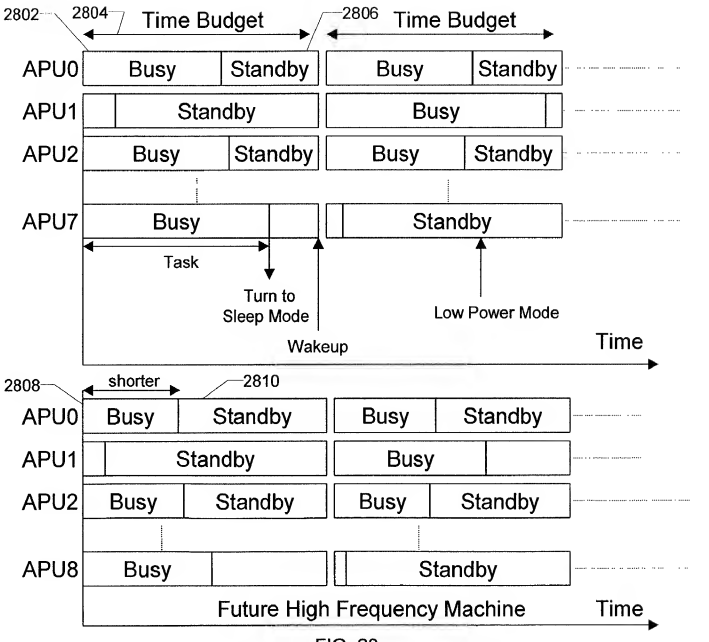
2802
2804
Time Budget
2806
Time Budget
APU0
Busy
Standby
Busy
Standby
APU1
Standby
Busy
APU2
Busy
Standby
Busy
Standby
APU7
Busy
Standby
Task
Turn to
Sleep Mode
Low Power Mode
Wakeup
Time
2808
shorter
2810
APU0
Busy
Standby
Busy
Standby
APU1
Standby
Busy
APU2
Busy
Standby
Busy
Standby
APU8
Busy
Standby
Future High Frequency Machine
Time

FIG. 28